UNIVERSITY OF AGRICULTURE

INSTITUTE FOR HUMAN RESOURCES DEVELOPMENT(INHURD)

DEPARTMENT OF COMPUTER SCIENCE

2009/2010 SECOND SEMESTER EXAMINATION

Course code: CSC424 Course Title: MINI AND MICRO COMPUTERS

Time Allowed: 2½ hours Instruction: Answer any FOUR questions

1a. What is meant by distributed computer system?
b. Describe and discuss the key merits of distributed computing.
c. What are the major drawbacks of distributed processing?
d. What is meant by process migration and what are its advantage?

2. Describe and discuss the following basic models and configurations of distributed systems:

a. Host-based (minicomputer) model

a. Processor pool model

b. Workstation Model

c. Integrated Model

3a. What is a parallel processing and what are its classification?

b. In a certain scientific computations it is necessary to perform the arithmetic operation $(A_i+B_i)(C_i+D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6.

c. Consider the multiplication of two 40 * 40 matrices using a vector processor.

i. How many product terms are there in each inner product and how many inner products must be evaluated?
ii. How many multiply-add operations are needed to calculate the product matrix?

4a. What is pipelining and how is it different from nonpipeline unit?

b. Draw a space time diagram for a six segment pipeline showing the time it takes to process eight tasks.

c. Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline.

5. Explain the following:

i. Vector Processing
ii. Vector operations
iii. Memory Interleaving
iv. Supercomputers
v. Array Processor

6a. A non pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?

b. The pipeline of the figure below has the following propagation times: 40ns for the operands to be read from memory into registers R1 and R2, 45ns for the signal to propagate through the multiplier, 5ns for the transfer into R3, and 15ns to add the two numbers into R5.

a. What is the minimum clock cycle time that can be used?
b. A nonpipeline system can perform the same operation by removing R3 and R4. How long will it take to multiply and add the operands without using the pipeline?
c. Calculate the speed up of the pipeline for 10 tasks and again for 100 tasks.
d. What is the maximum speed up that can be achieved?